Amendments to the Specification:

Please replace the paragraph starting on p. 2, line 9 with the following amended paragraph:

Figure 1 shows a block diagram of the R-CQICH channel generation structure provided by CDMA-2000 Release C. For full C/I updates, 4 bits per update are fed to a (12,4) block encoder 20 which produces a 12 bit output. The output of this is then fed to sequence repetition block 22 which repeats the sequence 1, 2 or 4 times as indicated above. For full C/I updates, the switch 25 is switched to connect the output of the sequence repetition 22 to the multiplier 26. The output of the sequence repetition 22 is then multiplied with multiplier 26 by the 8-symbol Walsh cover as indicated at 28. The 8-symbol Walsh cover will indicate which sector will transmit to the mobile on the forward link for the next slot. Finally, the output of the multiplier 26 is multiplied by a 16-symbol Walsh cover as indicated at 30. 96 symbols per slot are output by a multiplier 26. For differential C/I updates, the switch 25 is switched to connect the output of the symbol repetition 24 to the multiplier 26. For differential C/I updates, a single CQI symbol is input to symbol repetition function 24. This is in the form of 1 bit per 1.25 millisecond slot. This single bit is then simply repeated 12 times and output to multiplier 26. It can be seen that a given slot is either used to transmit a full C/I update or the differential C/I update.

Please replace the paragraph starting on p. 3, line 13 with the following amended paragraph:

According to one broad aspect, the invention provides a method of decoding M x N (symbols in which a first codeword of length N of a first set of K codewords has been spread by a second codeword of length M of a second set of L codewords, the first codeword identifying a first information and the second codeword identifying a second information, the method comprising: for each set of M consecutive symbols, performing a first parallel code multiplying operation by multiplying the M symbols by each of the L codewords of the second code, thereby producing L first output symbols, each of the L output first output symbols being associated with one of the L codewords; for each of at least one codewords of said set of L codewords: for a set of N consecutive first output symbols associated with the codeword, performing a respective second parallel code multiplying operation by multiplying the set of N consecutive first output symbols by each of the K codewords of the second code to produce a set of K second output symbols, each second output symbol being associated with one of the K codewords and with said

codeword of the set of said L codewords; determining an overall maximum of the second output symbols output of said second parallel code multiplying operations.

Please replace the paragraph starting on p. 6, line 1 with the following amended paragraph:

According to another broad aspect, the invention provides an apparatus for decoding M x N (symbols in which a first codeword of length N of a first set of K codewords has been spread by a second codeword of length M of a second set of L codewords, the first codeword identifying a first information and the second codeword identifying a second information, the apparatus comprising: a first parallel code multiplier which, for each set of M consecutive symbols, performs a first parallel code multiplying operation by multiplying the M symbols by each of the L codewords of the second code, thereby producing L first output symbols, each of the L output first output symbols being associated with one of the L codewords; a second parallel code multiplier which, for each of at least one codewords of said set of L codewords, performs: for a set of N consecutive first output symbols associated with the codeword, a respective second parallel code multiplying operation by multiplying the set of N consecutive first output symbols by each of the K codewords of the second code to produce a set of K second output symbols, each second output symbol being associated with one of the K codewords and with said codeword of the set of said L codewords; wherein an overall maximum of the second output symbols output of said second parallel code multiplying operations is selected.

Please replace the paragraph starting on p. 8, line 11 with the following amended paragraph:

Figure 2 is a block diagram of a straight forward decoding structure for the R-CQICH generated using the structure of Figure 1. The output 50 of an MRC (Maximum Ratio Combiner) is used to construct a vector of eight symbols at 52 which is then converted to parallel form with serial-to-parallel converter 54. The eight outputs of the serial-to-parallel converter 54 are input to an 8-FHT (Fast Hadamard Transform) 56. The 8-FHT 56 has 8 outputs indicated i = 1, i = 2,...,i = 8. The 8-FHT block 56 applies eight different Walsh covers to the output of the serial-to-parallel conversion 54. The maximum output of the 8-FHT 56 is selected at 58. This involves performing an energy accumulation for each output of the 8-FHT. Effectively this looks at the 8 outputs and identifies the channel number i of the channel having the largest energy. Then 12 symbols of the selected output are output at 60. The assumption at this point is that the sector for which the channel quality indicator was transmitted is the sector having the Walsh

code cover associated with output i of the eight possible outputs of the 8-FHT 56. Then, depending upon whether it is the full update which is being decoded or the differential update which is being decoded, one of paths 66 or 68 is followed. For the full update, a switch 65 is switched to connect the output of the multiplier 64 to the path 66, and sequence de-repetition is performed as a function of the number of times the full update was repeated (this being 1, 2 or 4 in the above-identified examples) with symbol de-repetition block 70. The output of this block is fed to a (12,4) block decoder 72 which then produces the full channel quality update at 74. Typically, this channel quality will be a carrier to interference ratio (C/I). For the differential updates, the switch 65 is switched to connect the output of the multiplier 64 to the path 68, and symbol de-repetition is again performed at 76. In this case, the de-repetition factor would be 12 for the above example. Then, the differential update block 78 simply determines using a threshold whether or not the update was an increase or a decrease in one example, a "one" might reflect a 0.5 dB differential increase, whereas a "zero" might mean a 0.5 dB differential decrease. Disadvantageously, with this solution, if the signal quality is poor, the wrong sector may be decoded.